(12) UK Patent Application (19) GB (11) 2 236 026 (13) A

(43) Date of A publication 20.03.1991

(21) Application No 8920743.5

(22) Date of filing 13.09.1989

(51) INT CL[5]
G01R 23/14, H03L 7/08

(52) UK CL (Edition K)
H3A AE ALX AM
G1U UR2302 UR2316
H3R RA8S RFDX
U1S S2135

(56) Documents cited
GB 1110398 A EP 0220895 A1

(58) Field of search
UK CL (Edition J) G1U UBF, H3A AE, H3R RFDC RFDX
INT CL[4] G01R 23/00

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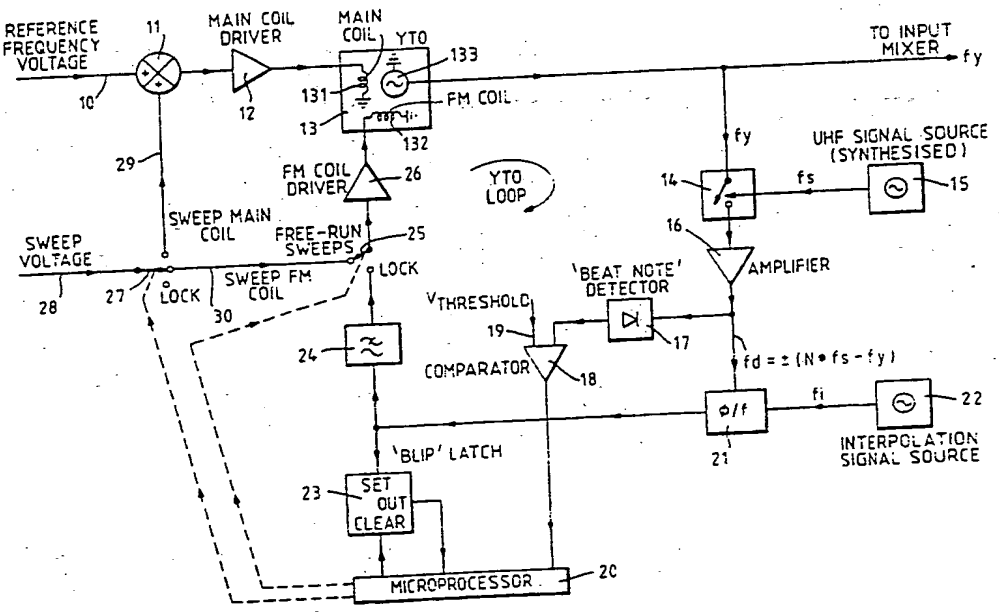
(54) Swept frequency signal generating circuit

(57) A swept frequency signal generating circuit for use as the first local oscillator of the superheterodyne receiver of a spectrum analyser, comprising: an oscillator 13 for generating the output signal; an arrangement for generating from a memory (not shown) a frequency control signal to tune the oscillator, the control signal being swept periodically over a predetermined range, a mixer 14 for mixing the output signal with a synthesised signal source 15 output to generate a difference frequency signal; an arrangement 17-19, 21, 22 for detecting the instant that the difference frequency crosses over a datum frequency; and an arrangement 20 responsive to the detecting arrangement and to the values of the datum frequency and the frequency of the synthesised signal source to provide an indication of the precise frequency of the output signal at the said instant of cross-over. A microprocessor 20 uses the cross-over frequency as a reference datum, determines the amplitude/frequency spectrum of an input signal and displays it. Two or more frequency cross-overs may be obtained by arranging the sources 15, 22 to be agile. For narrow sweeps, the oscillator 13 may be briefly controlled in a phase lock loop arrangement by applying to the oscillator 13 via a switch 25 the output of a phase comparator 21.



At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

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lower frequency oscillator whose frequency is known, perhaps by counting, so that the YTO frequency is synthesised from one oscillator or a combination of oscillators. Synthesised sweeps are practical over fairly narrow sweeps (perhaps up to several megahertz in range), but are limited by the tuning range of the lower frequency oscillators. On wider spans, the YTO is generally swept in its free-running (not phase-locked) state. On the widest of such spans this is acceptable from a measurement point of view in that coarser frequency resolution can more readily be tolerated. However, on the narrowest free-running spans generally used, inaccurate settings of the absolute frequency of an uncorrected oscillator, and its drift, cause objectionable frequency measurement errors.

The problem of frequency errors in the positioning of a free-running YTO swept over the narrower frequency spans, for example those from 5 to 50 MHz, is partly overcome by causing the YTO to phase-lock once in between free-running sweeps. Prior to the free-running sweep, the frequency of the YTO is coarse-steered towards the desired start frequency by applying a tuning voltage from a digital-to-analogue convertor (DAC) to the YTO driver. The YTO is then phase-locked to a harmonic of the lower frequency signal so that its frequency is known to be precisely at the desired starting frequency of the sweep. Since the coarse-steered YTO frequency will be in error, the phase-locked loop has to generate a correction voltage (the loop "error" voltage) which is proportional to the frequency error. This error voltage is stored and added to the coarse steering voltage, and the phase-locked loop is then broken; the YTO frequency will remain at the desired frequency. The sweep voltage is then applied to the YTO driver, and signal measurements are made in the knowledge that the start frequency is correct. This form of frequency correction can be made fast enough to be applied at the start of every sweep, thereby correcting for YTO drift such as may occur when its temperature is changing.

This method can only position one point on the sweep accurately, however, which limits the accuracy, especially where there is significant YTO drift.

The invention overcomes the problem by providing a swept frequency signal generating circuit comprising : an oscillator for generating the output signal; a memory; means for generating a frequency control signal from the memory to tune the oscillator, the

frequency represented by the control signal being swept periodically over a predetermined frequency range, a synthesised signal source; means for mixing the output signal with the synthesised signal source output to generate a difference frequency signal; means for detecting the instant that the difference frequency crosses over a datum frequency; and means responsive to the detecting means and to the values of the datum frequency and the frequency of the synthesised signal source to provide an indication of the precise frequency of the output signal at the said instant of cross-over. By responding to the cross-over of a frequency datum, it is possible to provide two or more precise frequency indications per sweep. No phase-locking time is involved. Moreover, the oscillator frequency may be determined accurately dynamically, while the sweep is in progress, which had not been possible hitherto.

The oscillator is preferably a YTO, and the detecting means preferably comprises a reference signal source and a phase comparator connected to compare the reference signal and the difference frequency signal.

For the selection of narrower sweeps with the YTO phase-locked, the circuit preferably has a switch for connecting the oscillator, the synthesised signal source, the mixing means and the phase comparator serially in a phase-locked loop.

Conveniently, the phase comparator is a phase/frequency comparator, allowing the system to distinguish between directions of sweep, to avoid frequency ambiguities in the interpretation of the value of the intermediate frequency.

The IF bandwidth of the mixing means, which is conveniently a sampling mixer generating a harmonic comb of discrete frequencies, is generally limited so that the difference frequency signal becomes insufficient at high difference frequencies to drive the phase comparator. Preferably, therefore, the circuit comprises a beat note detector responsive to the level of the difference frequency signal to provide an indication to the detecting means of whether the level is above a predetermined threshold corresponding to the level necessary for driving the phase comparator.

One swept frequency signal generating circuit embodying the invention will now be described, by way of example only, with reference to the accompanying drawing, which is a schematic circuit diagram.

The swept frequency signal generating circuit shown in the drawing forms part of the superheterodyne receiver of a spectrum analyser of conventional form. It is controlled by the central microprocessor 20 of the spectrum analyser, and it provides a swept frequency output signal f_y as the first local oscillator signal for the receiver. The analyser has a digital memory (not shown) for storing, amongst other data, the setting of a digital-to-analogue converter (DAC) whose output controls the voltage level used to drive the YTO 13, as described below.

The YTO 13 has an oscillator 133 whose output frequency is set by a main coil 131 and an FM coil 132 with respective drive amplifiers 12 and 26, as is well known. The main coil driver 12 has an input connected to a summer 11 which sums a reference frequency voltage 10 with whatever voltage level appears on a line 29 from a three-position switch 27. The FM coil driver 26 is connected via a two-position switch 25, under control of the microprocessor 20, either to a line 30 from the three-position switch 27, for free-running sweeps, or to a low-pass loop filter 24 to phase-lock a loop, to be described below. The three-position switch 27, which is also controlled by the microprocessor 20, connects an input sweep voltage consisting of a ramp waveform 28 selectively either to line 29 to apply the sweep to the main coil 131 for broad free-running sweeps, or to line 30 for narrower free-running sweeps, or to open circuit for phase-locked loop operation when the sweep voltage is not required.

The output signal f_y is sampled in a sampling mixer 14 by a U.H.F. synthesised signal at frequency f_s generated by a source 15. Very narrow pulses are generated at f_s in the mixer 14 to give a harmonic comb, one tooth of which (the nearest) mixes with the YTO signal f_y to produce a signal at the difference frequency f_d, within the range of intermediate frequencies of the mixer. Thus $f_y = N.f_s +/- f_d$, where N is an integer representing the harmonic number.

The difference signal f_d is amplified at 16, and its power level is detected by a "beat note" detector 17. A comparator 18 compares the power level with a predetermined threshold voltage level at 19 and provides a signal to the microprocessor indicative of the result of the comparison. The threshold level corresponds to that which is sufficient to drive a phase/frequency comparator 21 to which

the amplifier 16 is connected.

The phase/frequency comparator 21 compares the difference signal f_d and a signal f_i from an interpolation oscillator 22 at a frequency f_i which is lower than the frequency f_s. The interpolation signal frequency f_i is arranged to be well within the IF bandwidth of the sampling mixer 14. As the YTO is swept by the FM coil driver 26 under control of the sweep voltage 28, the differency frequency f_d changes. As it changes, frequency f_d can cross frequency f_i, at which instant the phase/frequency comparator output changes state. The direction of the change depends on the direction in which the difference frequency sweeps, thus removing the possible ambiguity between two values of the YTO frequency which both give rise to the same difference frequency f_d.

The instantaneous change of state of the output is recorded by setting a bistable "blip" latch 23. The output of the "blip" latch 23 is connected to the microprocessor 20 to indicate that the YTO frequency f_y has crossed a frequency datum, as will be described below. The latch is then cleared by the microprocessor.

The output of the phase/frequency comparator 21 indicative of the frequency error is also connected via the low pass loop filter 24 to the "lock" terminal of the two-position switch 25. This enables the YTO 13, sampling mixer 14, phase/frequency comparator 21 and loop filter 24 to be connected serially in a phase-locked loop, for operation in a conventional manner, for the narrowest sweeps only. In this mode, the "blip" latch is redundant.

The microprocessor 20 responds to the latch 23 output, the frequency settings f_s and f_i, the stored value of the reference frequency voltage on line 10 which provides coarse tuning, and the stored value of the sweep voltage 28, to determine a more accurate value of the YTO frequency f_y; it causes the input signal amplitude at each correct frequency value f_y to be displayed graphically on a screen.

In one method of frequency determination, for the narrower free-running sweeps, the microprocessor first sets up the UHF and interpolation signal sources appropriately for the sweep, and sets the reference frequency voltage 10 to tune the YTO close to a selected datum frequency, usually at the interpolation frequency $f_i + N.f_s$. The blip latch 23 is cleared. The DAC is then caused to sweep the YTO so that its frequency crosses the datum

frequency. The microprocessor records the timing of the cross-over, and records the instruction currently being processed by the DAC, corresponding to the sweep voltage sent to drive the YTO, at that instant of frequency cross-over. It therefore records the YTO drive parameter corresponding to a well-defined frequency.

The microprocessor then calibrates the frequency/time information obtained from analysing the input signal, using as a datum the cross-over point, determines the amplitude/frequency spectrum using a conventional algorithm, and displays the spectrum.

This gives only one datum point, and thus no greater accuracy than the previously-known system employing periodic phase-locking to set the frequency at a single datum frequency. However, it is an improvement in that it is faster, since no phase-locking time is required, and it is dynamic, establishing the YTO frequency whilst it is being swept, thus allowing dynamic errors such as lags in the YTO or its driving system to be taken into account.

In an improvement, two or more frequency cross-overs are contrived to occur in each sweep. This is possible if the lower frequency signal sources 15, 22 are sufficiently agile; the microprocessor 20 re-positions their frequencies during the sweep, so that multiple "blips" are recorded at corresponding precise frequency datum prints. After each "blip" is recorded, the latch 23 is cleared, as before.

In an alternative system, the "blip" technique is used to set up the start frequency of each sweep, by scanning the reference frequency voltage 10 until frequency cross-over is recorded.

In a further alternative, the "blip" technique is used to trigger the gathering of data for display, i.e. to set the instant after which data are collected for display. This ensures that the frequency sweep begins at a datum frequency.

Other possibilities are envisaged, for example the use of one or more frequency cross-over points just outside the desired frequency sweep span, and interpolating to determine a datum frequency within the span and/or to determine a precise value for the sweep gain to compensate for YTO drift.

CLAIMS

1. A swept frequency signal generating circuit comprising : an oscillator for generating the output signal; a memory; means for generating from the memory a frequency control signal to tune the oscillator, the frequency represented by the control signal being swept periodically over a predetermined frequency range, a synthesised signal source; means for mixing the output signal with the synthesised signal source output to generate a difference frequency signal; means for detecting the instant that the difference frequency crosses over a datum frequency; and means responsive to the detecting means and to the values of the datum frequency and the frequency of the synthesised signal source to provide an indication of the precise frequency of the output signal at the said instant of cross-over.

2. A circuit according to Claim 1, in which the detecting means comprises a reference signal source and a phase comparator connected to compare the reference signal and the difference frequency signal.

3. A circuit according to Claim 2, comprising a switch for connecting the oscillator, the synthesised signal source, the mixing means and the phase comparator serially in a phase-locked loop.

4. A circuit according to Claim 2 or 3, in which the phase comparator is a phase/frequency comparator.

5. A circuit according to Claim 2, 3 or 4, comprising a beat note detector responsive to the level of the difference frequency signal to provide an indication to the detecting means of whether the level is above a predetermined threshold corresponding to the level necessary for driving the phase comparator.

6. A circuit according to any preceding claim, in which the mixing means comprises a sampling mixer which generates from the synthesised signal a stream of narrow pulses defining a harmonic comb of discrete frequencies of which one is subtracted from the frequency of the output signal to produce the difference frequency.

7. A circuit according to any preceding claim, in which the

oscillator is a YIG-tuned oscillator.

8. A superheterodyne receiver comprising a swept frequency signal generating circuit according to any preceding claim, of which the said oscillator constitutes the first local oscillator of the receiver.

9. A spectrum analyser comprising a superheterodyne receiver according to Claim 8, a display for displaying the amplitude against frequency of a received input signal, and a main processing block for driving the display including data processing means responsive to the said indication of the precise frequency to calibrate the signal sent to the display.

10. A signal generating circuit substantially as described herein with reference to the accompanying drawing.

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